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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,738	03/06/2002	Stewart R. Wyatt	10018462-1	8159
7590	10/06/2005		EXAMINER	
HEWLETT-PACKARD COMPANY Intellectual Property Administration P.O. Box 272400 Fort Collins, CO 80527-2400			LAMARRE, GUY J	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,738	WYATT ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 01 August 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 03/06/02 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

* A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1 Aug. 2005 has been entered.

- . This office action is in response to Applicants' amendment of 1 Aug. 2005.
- . **Claims 1, 9, 15 and 18-19** are amended; **Claims 22-23** are added. **Claims 1-23** remain pending.
- . The objections and rejections under 35 USC 112 of record are withdrawn in response to Applicants' amendment.
- . The prior art claim rejections of record are maintained in response to Applicants' amendment.

Response to Arguments

* Applicants' arguments have been fully considered, but are not deemed persuasive because the claimed erasure feature is disclosed by **Glover** as underlined in para. 3 below, and because **Glover** does not restrict error code capability setting threshold as alleged by applicants.

a. Applicants' arguments, re: threshold setting on page 13, are not persuasive because:

* Natural limitations of a system cannot dictate limitation or 'threshold:' the limitations of a system are a design factor determined at the planning stage, as admitted by Applicants' specification, e.g., 'In designing error correction code and circuitry, a decision is made as to the number of errors that are likely to be seen. This decision determines how many parity bytes should be added in order to correct the errors. The parity bytes add cost to the system by occupying storage

space that is not available for storing the user's data. Therefore, it would make sense to minimize the parity bytes as much as possible. However, if the number of errors in a codeword is greater than what the system is capable of correcting, then the codeword will be uncorrectable and cannot be recovered. Even worse, the original data could be unknowingly corrupted. This is called an undetected error. By analyzing the number of full errors and erasures, the present invention may be used to optimize the number of parity bytes for a certain number of bytes of the entire codeword.'

* 'Not specifically described in detail' does imply 'not described at all;'

Applicants admit/remark/concede, at page 11 last para., that **Glover** provides for 1st ECC at the sector level and for 2nd ECC at the track level when error limits/thresholds are exceeded.

Examiner maintains that this is equivalent to the claimed invention because 1st level ECC is effected when 1st threshold/limit is exceeded (XOR or 1st level RS coding), 2nd level ECC may be executed if 1st threshold/limit is exceeded thereby requiring a more robust RS code, 3rd level corrective step is also possible for completely 'unreadable sector....'

b. Applicants' arguments, re: **Glover/Inouie/Zook**, at page 13 et seq., are not persuasive because, since **Glover** discloses data transfer pausing means, **Inouie** or **Zook** do not have to suggest same.

Therefore, the prior art of record does set plural error/erasure levels or thresholds for the pausing of data transfer.

Claim Rejections - 35 USC § 102

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by **Glover** (US Patent No. 5,751,733; 12 May 1998).

As per Claims 1-23, **Glover** discloses an equivalent data transfer pausing procedure and configuration during storage access or data verification (*'Verify commands of the prior art have some limitations in certain test environments, per applicants' spec.'*) wherein storage comprises disk storage,

memory cards, in “*Interleaved redundancy sector for correcting an unrecoverable sector in a disc storage device,*” as depicted in Fig. 1c and described in col. 6 line 10 et seq. wherein, when an error threshold is reached, a ‘storage system pauses the data transfer and executes the track level error correction steps to recover the lost sector using the redundancy sector...’ along with the use of erasure pointers.

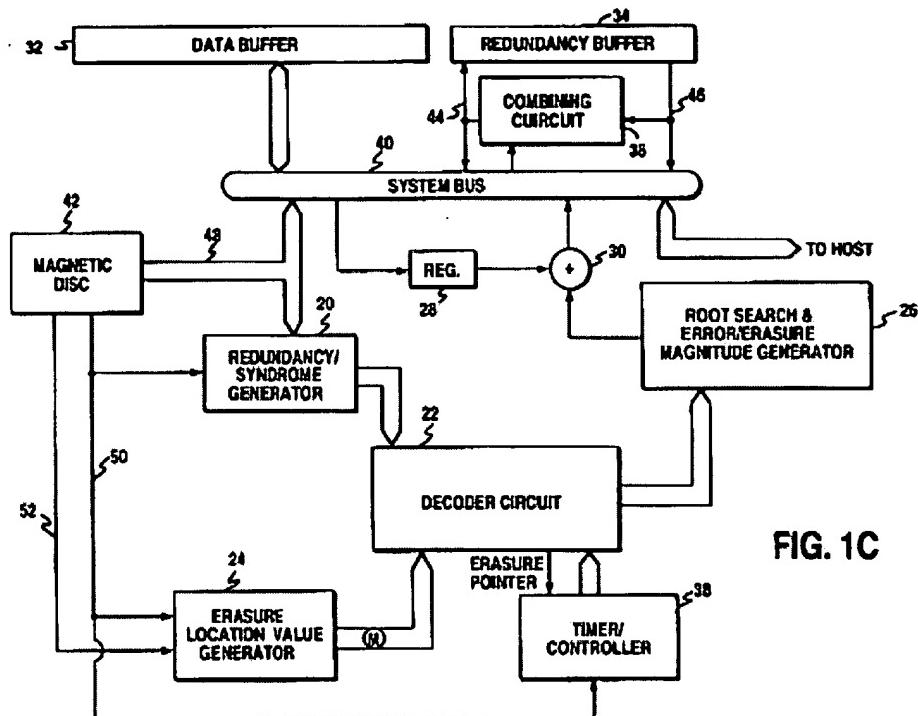


FIG. 1C

Glover discloses the claimed system for pausing data transfer e.g., in col. 7 line 24 et seq., and the verify command comprising: full error/erasure tracking means (col. 4 line 2 and Fig. 1c: **Numerals 20, 24, 26**), sparing means in Fig. 4c: **Numeral 216**), error condition threshold setting means along with compare means to evaluate match or mismatch with ECC error capability, such as ECC error capability comprising means to detect/correct full errors and erasures, e.g., in col. 7 line 22 et seq., data recovery at e.g., in Figs. 3c, 4b, 6a-6c and col. 7 lines 28, 30 et seq., write verify operation/command means in Figs. 4e-4f, 6a-6c, e.g., “*As mentioned above, there are two situations where a data sector on the disc may become unrecoverable. First, the sector may become entirely unreadable due to an inability to synchronize to the sector data (because, for*

example, the preamble 6 or sync mark 8 have been corrupted by a defect on the medium). The other possibility is that the sector becomes uncorrectable; that is, the number of hard errors exceeds the error correction capability of the sector level ECS. In these situations, the storage system pauses the data transfer and executes the track level error correction steps to recover the lost sector using the redundancy sector.

...The prior art track level error correction systems are limited to correcting only one unrecoverable data sector per track because the redundancy sector is generated as the byte XOR of the respective data bytes in the data sectors. This severely limits the benefit of using a redundancy sector, especially in cases where a burst error spans two sectors, thereby rendering both sectors unrecoverable at the sector level and at the track level. The present invention improves the error correction capability of the track level ECS by dividing a sector into three interleaved codewords and generating the redundancy sector by combining the respective symbols in each codeword according to a predetermined error correction operation (e.g., byte XOR).....This aspect of the present invention is understood with reference to FIG. 9 which shows each data sector divided into three codewords, and the codewords being combined (XORed) across three interleaves (designated INTLV 0, INTLV 1 and INTLV 2) to generate an interleaved redundancy sector. The data sector itself is interleaved to generate the three codewords; that is, symbol 0 is placed in the first codeword, symbol 1 is placed in the second codeword, symbol 2 is placed in the third codeword, symbol 3 is placed in the first codeword, etc.. Then, sector level redundancy is generated for each of the three codewords and stored in the data sector. Upon read back, the data symbols read from the disc are de-interleaved into the three codewords and each codeword is processed by the sector level ECS separately. In this manner, the sector level ECS can generate an erasure pointer corresponding to an unrecoverable codeword within a sector (i.e., an unrecoverable codeword in INTLV0, INTLV1 or INTLV2). Using the erasure pointers, the track level ECS is capable of correcting a single unrecoverable codeword in each interleave, and the unrecoverable codewords can occur in different sectors. Thus, using the interleave technique of the present invention, the track level ECS is capable of correcting up to three unrecoverable data sectors containing a single uncorrectable codeword in separate interleaves.

...Preferably, the redundancy sector is generated according to: 2.sup.m --the sum modulo 2.sup.m of the respective codeword symbols in an interleave (i.e., INTLV0, INTLV1 or INTLV2), where m is the size in bits of a codeword symbol. Then, the track level error syndromes for correcting a codeword are generated as the sum modulo 2.sup.m of the respective codeword symbols in an interleave, including the redundancy sector codeword. The error syndromes are then used to correct a data codeword uncorrectable at the sector level that corresponds to the erasure pointer generated by the sector level ECS. That is, the erasure pointer identifies the sector and interleave location of the uncorrectable codeword, and the track level ECS uses the erasure pointers to correct up to three codewords in separate interleaves which can occur in three different sectors.'

Claim Rejections - 35 USC ' 103

.. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Glover** and respective **Inouie et al.** (US Patent No. 5,712,861) and **Zook** (US Patent No. 5,600,662).

As per Claims 1-23, Glover substantially discloses an equivalent data transfer pausing procedure and configuration during storage access or data verification, wherein storage comprises disk storage, memory cards. **Not specifically described in detail** by **Glover** is the step whereby an error threshold feature is selected for a code. **However Inouie**, in an analogous art, discloses such feature. {See **Inouie**, Id., col. 35 line 44 et seq.; or **Zook** at col. 27 line 47, col. 29 line 55 et seq.}. **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Glover** by including therein an error threshold feature as taught by **Inouie** or **Zook**, because such modification would provide the procedure **Glover** with a method whereby system hardware can be optimized. {See **Inouie**, Id., col. 35 line 44 et seq.; **Zook** at col. 27 line 47, col. 29 line 55 et seq.}

Conclusion

- **Applicants** are invited to call **Examiner** for discussing possible allowable subject matter.
- Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Guy J. Lamarre, P.E
Primary Examiner
10/3/2005
